Low Dark Current 1024x1280 InGaAs PIN Arrays

Ping Yuan*, James Chang, Joseph C. Boisvert, and Nasser Karam
Spectrolab Inc., a Boeing Company, 12500 Gladstone Ave., Sylmar, CA, USA 91342

ABSTRACT

Photon counting imaging applications requires low noise from both detector and readout integrated circuit (ROIC) arrays. In order to retain the photon-counting-level sensitivity, a long integration time has to be employed and the dark current has to be minimized. It is well known that the PIN dark current is sensitive to temperature and a dark current density of 0.5 nA/cm^2 was demonstrated at 7 ºC previously. In order to restrain the size, weight, and power consumption (SWaP) of cameras for persistent large-area surveillance on small platforms, it is critical to develop large format PIN arrays with small pitch and low dark current density at higher operation temperatures.

Recently Spectrolab has grown, fabricated and tested 1024x1280 InGaAs PIN arrays with 12.5 µm pitch and achieved 0.7 nA/cm^2 dark current density at 15 °C. Based on our previous low-dark-current PIN designs, the improvements were focused on 1) the epitaxial material design and growth control; and 2) PIN device structure to minimize the perimeter leakage current and junction diffusion current. We will present characterization data and analyses that illustrate the contribution of various dark current mechanisms.

1. INTRODUCTION AND BACKGROUND

For airborne Intelligence, Surveillance, and Reconnaissance (ISR) missions in the Short-Wave Infrared (SWIR) band, it is essential to develop large format focal plane arrays (FPAs) to cover a larger area with good image quality and small camera SWaP. The image quality is largely determined by the pixel sensitivity, quantum efficiency, fill factor, dynamic range, array format and defect counts. Because the quantum efficiency and fill factor are close to 1 in InGaAs PIN structures, the effort of pixel sensitivity improvement is focused on the pixel dark current. In order to achieve low dark current, PIN arrays are normally operated at reduced temperature to suppress the junction diffusion current and generation-recombination (G-R) current. However, since the focal plan array (FPA) temperature control consumes most of the camera power, it is highly desirable to keep a higher operating temperature while maintaining a limited pixel dark current to restrain the camera power consumption.

For fine image resolution and large field of view (FOV), another focus in SWIR FPA development is large format with small pitch. In order to constrain the size and weight of optics and camera with large format arrays, small pixel pitch becomes critical. A small pitch also helps to reduce the pixel dark current. However, as the pitch decreases, the PN junction inevitably becomes shorter, and the contributions from tunneling and surface leakage become more important and impose challenges to further dark current decrease. In this paper, we will demonstrate a 1024x1280 InGaAs PIN array with 12.5 µm pitch and 0.7 nA/cm^2 at 15 ºC.

2. INGAAS PIN ARRAY

For applications around 1.55 µm wavelength, the classic Zn-diffused planar InGaAs/InP PIN makes a good baseline design for its excellent crystal quality, surface InP surface junction, and proper bandgap, which all help to achieve very low dark current. As shown in Figure 1, the diffused P-well reaches the InGaAs/InP hetero-interface and part of the assigned pixel footprint. Under the operation condition, with is about 150 mV, the depletion region will extend a little more, but there is a considerable undepleted area between

* Email: ping.yuan@boeing.com; Tel: 818 898 7578; Fax : 818 838 7474.

pixels Because the electron diffusion length is much longer than the pixel pitch in these undepleted N materials, almost all the photo-generated carriers will be transported to and collected by the nearest pixels. So, the structure can conveniently achieve nearly 100% fill factor and >80% quantum efficiency with sufficient InGaAs thickness.

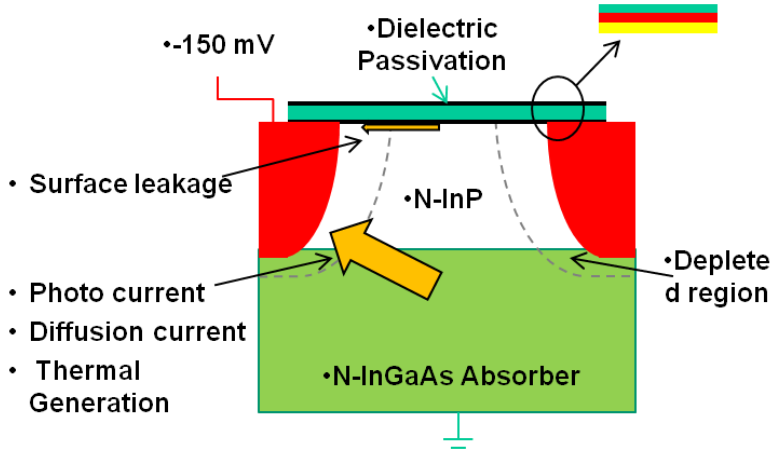


Figure 1 The Planar InGaAs/InP planar structure employed by Spectrolab. Three major dark current sources were illustrated. In order to suppress the surface leakage, especially for small pitch arrays, Spectrolab developed a proprietary surface passivation.

A portion of a processed array with 12.5 µm pitch is shown in Figure 2. Because there is no mesa etch, the pitch could be reduced further in process if the surface leakage and tunneling currents can be in control.

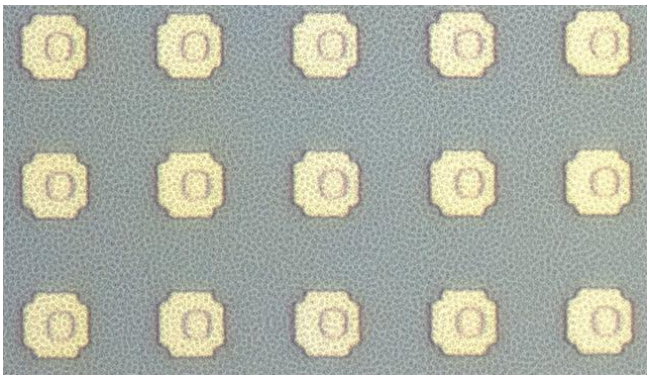


Figure 2 A portion of a processed array with 12.5 µm pitch.

As mentioned above, for the concerns of pixel sensitivity, the dark current has to be suppressed. There are four major dark current sources in the diffused planar PIN structure: junction diffusion current J_D, G-R current J_{GR}, tunneling current J_T, and surface leakage J_L. The temperature dependence of J_D and J_{GR} is well known as[1];

$$J_D \propto (e^{\frac{E_a}{kT}} - 1)$$
$$J_{GR} \propto (e^{\frac{E_a}{2kT}} - 1) \qquad \text{Eq. 1}$$

where E_a is the activation energy. The temperature dependence of the four sources and their combination is shown in Figure 3. As pitch decreases, the junction width becomes shorter and the peak electric field in the junction becomes higher. All these factors will increase the contribution of J_T and J_L in the total dark current. Because they are insensitive to temperature, at certain point, they have to be carefully suppressed

before considering lowering the temperature to reduce J_D and J_{GR}. This makes one of the major challenges to reduce the array pitch further.

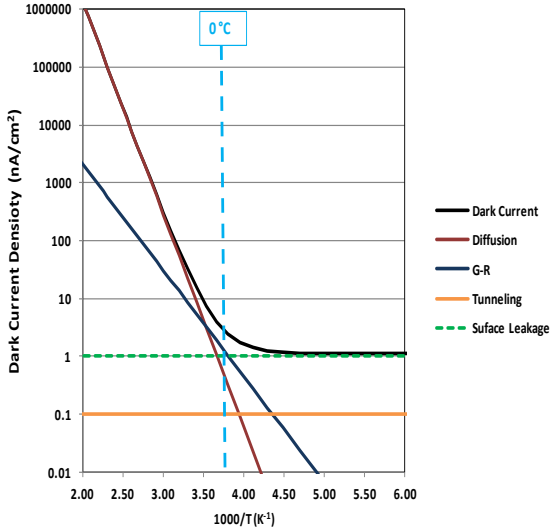


Figure 3 The temperature dependence of the four dark current sources and their combination.

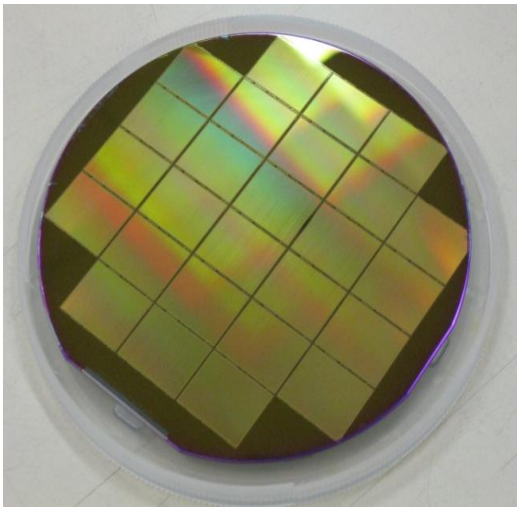


Figure 4 A processed 100 mm InP wafer with 26 1024x1280 InGaAs/InP PIN arrays with 12.5 µm pitch.

3. PROCESS

The epitaxial structure shown in Figure 1 is grown on 100 mm InP substrates in Spectrolab production Metal-Organic Vapor Phase Epitaxy (MOVPE) reactors. The Zn diffusion is performed in the same reactor to form the Zn well for each pixel masked by a patterned dielectric layer. As shown in Figure 1, the diffusion front is controlled to the InGaAs/InP hetero-interface. In order to control the alignment error of the small device features and minimize the defects introduced by photolithography, a GCA 6300 stepper was employed for the array process.

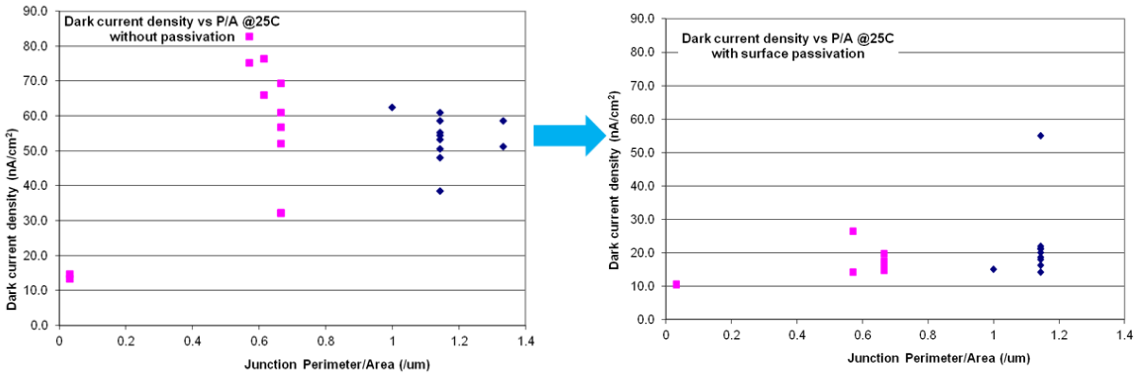
After the P-well diffusion, there is a surface PN-junction formed around each pixel. In order to suppress the surface leakage through this junction, the InGaAs contact layer is etched away so that this junction is in InP

with wider bandgap. In the pursuit of extremely low dark current, this junction has to be carefully passivated. In order to separate this component from other dark current sources, we can consider the surface leakage current as $I_P P$, where P is the total junction peripheral length of pixels, and bulk dark current as $I_B A$, where A is the total junction area of pixels. Then the total dark current density I_{DK} can be expressed as

$$I_{DK} = I_P \frac{P}{A} + I_B \qquad \text{Eq. 2}$$

By measuring the dark current density of different devices with different P/A values, we can distinguish the contribution of I_P and I_B from the total dark current.

In Figure 5, the contribution of surface leakage and the impact of the Spectrolab surface passivation were demonstrated with and without the surface passivation on the same PIN wafer. Without the surface passivation, the dark current is dominated by the surface leakage, which makes the total dark current more than 50 nA/cm^2 at 25 ºC and insensitive to temperature. After passivation, the dark current of most devices is reduced to less than 20 nA/cm^2. Without the inference of surface leakage, we eventually were able to optimize the device structure and reduced the total dark current to 2.0 nA/cm^2 at 25 ºC and 0.7 nA/cm^2 at 15 ºC.



(a) (b)

Figure 5 The dark current density vs junction P/A chart of an early PIN wafer without (a) and with (b) Spectrolab proprietary surface passivation measured at 25 ºC. Without the surface passivation, the dark current is dominated by the surface leakage, which makes the total dark current more than 50 nA/cm^2 and insensitive to temperature. After passivation, the dark current of most of devices is reduced to less than 20 nA/cm^2.

4. SPECTOLAB LOW DARK CURRENT 1024X1280 PIN ARRAY

Because the dark current of a single pixel is in the fA level, we connected about 200 pixels to increase the total dark current to sub pA level for the convenience in measurement. The test structure is shown in Figure 6. Because the minority carriers have much longer diffusion length than the pixel pitch, a guard ring is employed to block the carriers from outside the pixel footprint and simulate the electric environment of pixels in a large array. However, because any defect in this group will greatly deteriorate the average performance, the group size has to be limited and the result may vary in a larger range.

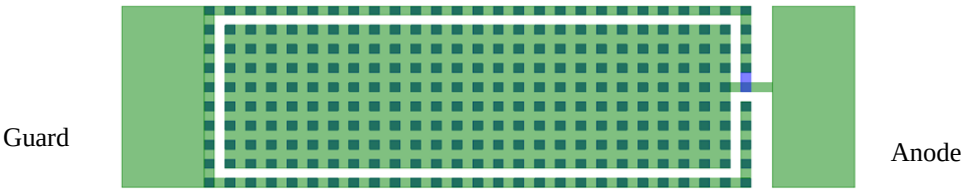


Figure 6 The mask layout of a test structure with 200 pixels. All the pixels in the anode and guard are designed the same except the metal connection. The deep and light blue regions are diffused. The green regions are metal.

Based on the above observation, Spectrolab developed a proprietary passivation process for dense planar InGaAs/InP PIN arrays. After suppressing the surface leakage, Spectrolab fine tuned the epitaxial structure and optimized the next major dark current source, junction diffusion current, at 150 mV. The dark current density as a function of bias of the recent 12.5 µm pixels is shown in Figure 7. They were measured with the test structure shown in Figure 6 at 15 ºC and 25 ºC. At 15 ºC, the dark current density is about 0.7 nA/cm2 at 150 mV bias. At 25 ºC, it is about 2.0 nA/cm^2 under the same bias condition. Because the FPA cooling consumes most of the camera power, this PIN array makes it possible to operate a SWIR camera with much lower power and achieve the same sensitivity as achieved at 7 ºC before.

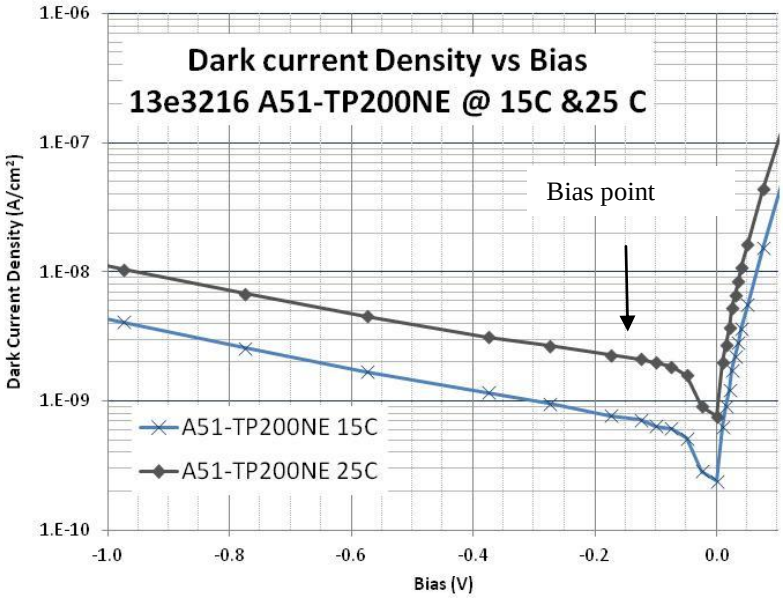


Figure 7 Dark current density vs bias. The curves were measured with 200 pixel test structure at 15 ºC and 25 ºC. At 15 ºC, the dark current density is about 0.7 nA/cm2 at 150 mV bias. At 25 ºC, it is about 2.0 nA/cm^2.

As shown in Figure 7, the two curves are nearly parallel to each other with a ratio of about 3. Because the tunneling current is sensitive to bias but and insensitive to temperature, this phenomenon indicts the dominance of temperature sensitive components, J_D and J_{GR}, in the current design. With Eq. 1, an effective activation energy of 0.29 eV can be easily calculated with this ratio. Because the J_{GR} is from the whole pixel footprint and the electron diffusion current is only from the depleted region, the contribution of J_{GR} is overweighed in this simple estimate. On the other hand, the dark current density does not show obvious dependence on P/A and indicates that the surface leakage was successfully suppressed. This is also consistent with the above analysis with the two parallel curves in Figure 7. Therefore, the junction diffusion

current is still dominant with some minor contribution from generation-recombination current in the demonstrated PIN pixel design.

Based on the above analysis, the further dark current improvement of 12.5 μm PIN pixels at Spectrolab will be focused on the reduction of junction diffusion current, which involves fine control and optimization of junction diffusion depth, epitaxial doping levels, and crystal quality. For smaller pitches than 12.5 μm, the tunneling and surface leakage currents will become more important. Additional efforts will be made on surface passivation improvement and process simplification.

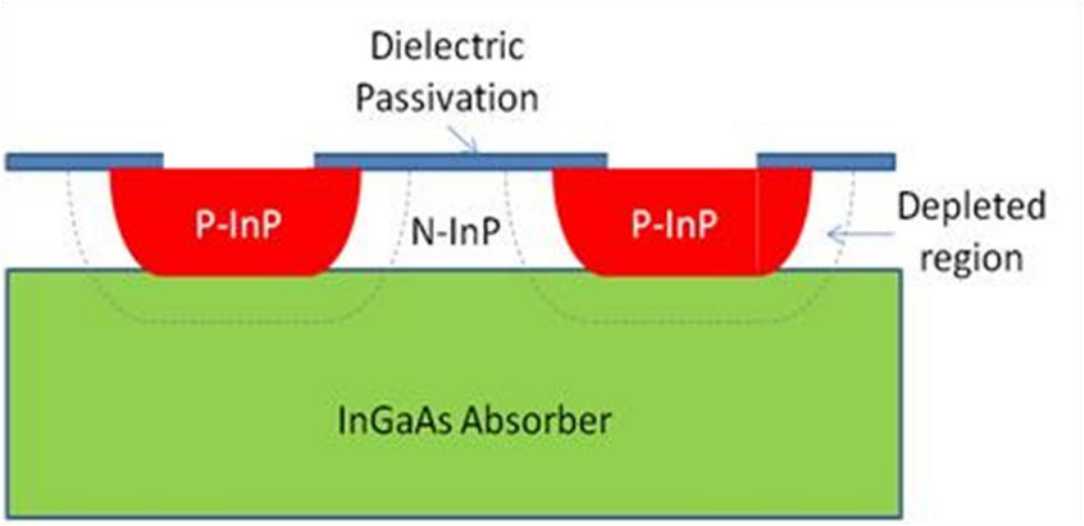


Figure 8 Cross section of two typical Spectrolab PIN pixels.

5. SUMMARY

For SWIR imaging applications, Spectrolab developed high performance 1024x1280 InGaAs/InP PIN arrays with 12.5 μm pitch. At 150 mV bias, a dark current density of 2.0 nA/cm^2 was demonstrated at 25 ºC, while it can be reduced to 0.7 nA/cm^2 at 15 ºC. The pixel capacitance is controlled under 30 fF at the operating condition. Analysis shows the junction diffusion current is still the dominant dark current source. Spectrolab will continue this effort to achieve lower dark current/higher operating temperature and smaller pixel pitches.

REFERENCES

[1] S.M.Sze, *Physics of Semiconductor Devices*, 2nd Edition, pp. 87-94, Wiley-Interscience, New York, 1981.